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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/695,311	10/25/2000	Minoru Oohira	198778US2DIV	2441

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EXAMINER
JONES, JOSETTA I

ART UNIT	PAPER NUMBER
2812	9

DATE MAILED: 12/05/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/695,311	OOHIRA ET AL.	
	Examiner	Art Unit	
	Josetta I. Jones	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *8-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-14* is/are allowed.

6)☒ Claim(s) *8-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

In response to applicant's request for continued examination, the allowance is withdrawn and claims 8-13 are rejected based upon the following rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haghiri-Tehrani, U.S. Patent No. 5,756,379 in view of Fjelstad, U.S. Patent No. 6,001,671.

With regard to claim 8, Haghiri-Tehrani discloses forming a die bond pad and wire bond pads by fastening electrically conductive metal sheets at specified positions on the back of an insulating sheet and making apertures in the insulating sheet on the metal sheets (see column 3, lines 26-28 and figures 4 and 5); packaging for fastening the back of the discrete semiconductor element to the die bond pad and electrically connecting the electrodes of the discrete semiconductor elements on the wire bond pads (see column 4, lines 27-29 and figures 6 and 7); sealing the discrete semiconductor element installed on the insulating sheet with an integral sealing resin by

sealing the packaging surface of the insulating sheet with the resin (see column 4, lines 39-41 and figures 6 and 7).

Haghiri-Tehrani fails to disclose forming a plurality of sets of die bond and wire pond pads (and the subsequent formation of a plurality of discrete semiconductor elements); and dividing the sealing resin into discrete semiconductor devices by cutting off the sealing resin around the discrete semiconductor devices by cutting off the sealing resin around the discrete semiconductor elements.

Fjelstad discloses forming a plurality of sets of die bond and wire pond pads (and the subsequent formation of a plurality of discrete semiconductor elements); and dividing the sealing resin into discrete semiconductor devices by cutting off the sealing. resin around the discrete semiconductor devices by cutting off the sealing resin around the discrete semiconductor elements (see column 4, lines 1-4 and column 5, lines 10-11). It would have been obvious to one skilled in the art at the time of the invention to form a plurality of discrete semiconductor elements and divide them after assembling the package because it is cost effective to produce a numerous semiconductor elements on a wafer and then to divide the wafer into discrete devices.

With regard to claim 9, Haghiri-Tehrani discloses wherein the step of packaging . . . also includes (sic) a step of fastening the back side electrode of the discrete semiconductor device onto the die bond pad to electrically connect the die bond pad and the back side electrode (see column 4, lines 27-39). It would have been obvious to one skilled in the art at the time of the invention to fasten the back side electrode of the discrete semiconductor device onto the die bond pad to electrically connect the die

bond pad and the back side electrode because fastening the discrete semiconductor to the die bond pad promotes the electrical connection of the die and the electrodes.

With regard to claim 10, Haghiri-Tehrani fails to disclose wherein the dividing step also be a step of cutting off the sealing resin around a plurality of discrete semiconductor elements grouped as a single body, to obtain the discrete semiconductor device wherein the plurality of discrete semiconductor elements are sealed with the integral resin (see figure 5H). Fjelstad discloses wherein the dividing step also be a step of cutting off the sealing resin around a plurality of discrete semiconductor elements grouped as a single body, to obtain the discrete semiconductor device wherein the plurality of discrete semiconductor elements are sealed with the integral resin. It would have been obvious to one skilled in the art at the time of the invention to obtain a discrete semiconductor device by cutting of the sealing resin around the plurality of discrete semiconductor elements because it is well known to separate a plurality of semiconductor devices into discrete semiconductor elements.

Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroyuki, Japanese Patent No. 5129473 in view of Fjelstad, U.S. Patent No. 6,001,671.

With regard to claim 8, Hiroyuki discloses forming a die bond pad and wiring bond pads by fastening electrically conductive metal sheets at specified positions on the back of an insulating sheet and making apertures in the insulating sheet on the metal sheets (see page 11, paragraph 0012, lines 3-5, 29-34); packaging for fastening the back of the discrete semiconductor elements on the die bond pads and electrically

connecting the electrodes of the discrete semiconductor elements and the wire bond pads (see page 11, paragraph 0012, lines 32-38 and figure 7B); sealing the discrete semiconductor element installed on the insulating sheet with an integral sealing resin by sealing the packaging surface of the insulating sheet with the resin (see page 11, paragraph 0012, lines 38-40).

With regard to claim 8, Hiroyuki fails to disclose forming a plurality of sets of die bond and wire pond pads (and the subsequent formation of a plurality of discrete semiconductor elements); and dividing the sealing resin into discrete semiconductor devices by cutting off the sealing resin around the discrete semiconductor devices by cutting off the sealing resin around the discrete semiconductor elements.

Fjelstad discloses forming a plurality of sets of die bond and wire pond pads (and the subsequent formation of a plurality of discrete semiconductor elements); and dividing the sealing resin into discrete semiconductor devices by cutting off the sealing. resin around the discrete semiconductor devices by cutting off the sealing resin around the discrete semiconductor elements (see column 4, lines 1-4 and column 5, lines 10-11). It would have been obvious to one skilled in the art at the time of the invention to form a plurality of discrete semiconductor elements and divide them after assembling the package because it is cost effective to produce a numerous semiconductor elements on a wafer and then to divide the wafer into discrete devices.

With regard to claim 10, Hiroyuki fails to disclose wherein the dividing step also be a step of cutting off the sealing resin around a plurality of discrete semiconductor elements grouped as a single body, to obtain the discrete semiconductor device

wherein the plurality of discrete semiconductor elements are sealed with the integral resin (see figure 5H). Fjelstad discloses wherein the dividing step also be a step of cutting off the sealing resin around a plurality of discrete semiconductor elements grouped as a single body, to obtain the discrete semiconductor device wherein the plurality of discrete semiconductor elements are sealed with the integral resin. It would have been obvious to one skilled in the art at the time of the invention to obtain a discrete semiconductor device by cutting of the sealing resin around the plurality of discrete semiconductor elements because it is well known to separate a plurality of semiconductor devices into discrete semiconductor elements.

Allowable Subject Matter

Claims 11-14 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose a cut-off step of cutting off the metal sheet by cutting therein from the back thereby to turn the metal sheet into die bond pads and wire bond pads which are arranged at intervals.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Steffen, U.S. Patent No. 5,041,395.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Josetta I. Jones whose telephone number is 703-308-

5871. The examiner can normally be reached on M-F 9:00-6:30 and alternating Fridays 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John F. Niebling can be reached on 703-308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-3432 for regular communications and 703-305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Josetta I. Jones
November 21, 2001

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800